

## REMARKS

The Office Action dated November 4, 2004 has been received and reviewed by the applicant. Claims 1-6 are in the application. Claims 1-5 stand rejected and claim 6 stands objected to as being dependent upon a rejected base claim. Claim 1 is amended. Reconsideration is respectfully requested.

Claims 1-5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,115,458, Burkey et al., in view of USPN 4,468,684, Esser et al. In response, claim 1 is amended to include "applying, at a first time period, a first set of voltages to the phases of the gate electrodes of the vertical shift registers sufficient to accumulate holes *substantially at a surface* of the image sensor in the vertical shift register, beneath each gate electrode." Support for the amendment is on page 13, line 9. In contrast, Esser et al. disclose at column 4, lines 56-58 that the "potential minima in which charge packets consisting of holes can be stored are formed in the p-type layer 3 at some distance from the surface." This teaches the opposite of the claimed invention. The claimed invention includes the advantage of reducing dark current and Esser et al. is completely silent on dark current. In addition, Esser et al. do not disclose an interline CCD which is discussed in detail hereinbelow.

Claim 1 is also amended to include having a "an interline CCD image sensor." In contrast, the Burkey disclosure will not function efficiently on an interline CCD (which are primarily fabricated on a n-type substrate) as discussed on page 6, lines 17 through page 7, line 5 of the present invention. There it states:

*The typical path for such hole charge removal or replacement is via a p-doped region such as the channel stop. For large devices, the net charge that must be moved in this way is significantly impeded by the relatively high resistance of the p-type regions. While this is true for any CCD operating in accumulation mode, this is a particularly troublesome problem for devices which are fabricated in deeply diffused p-doped regions on an n-type substrate. The problem becomes more severe as the area of the devices are made larger. This deeply diffused p-type region, referred to as a p-well, is typically isolated or only weakly connected with surface p-regions such as channel stops. The total amount of charge which must be drained off during the time one of the gates is in depletion is  $nQ$ , where  $n$  is the total number of pixels in the image sensor. During the time required to drain off the excess hole charge, the local value of the p-well bias moves, particularly in the central regions of the device, creating an undesirable biasing which leads to poor imaging properties for the device. This undesirable potential variation is sometimes referred to as p-well bounce. There is, thus, a shortcoming within the prior art in*

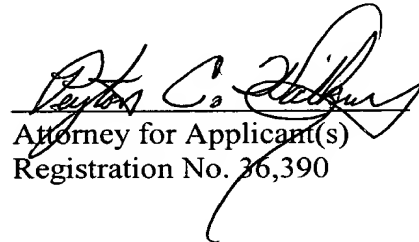
*avoiding p-well bounce when attempting to employ accumulation mode clocking.*

Therefore, it is respectfully submitted that Esser et al. and Burkey et al. do not individually or collectively teach or suggest the claimed invention.

Should the Examiner consider that additional amendments are necessary to place the application in condition for allowance, the favor is requested of a telephone call to the undersigned counsel for the purpose of discussing such amendments.

For the reasons set forth above, it is believed that the application is in condition for allowance. Accordingly, reconsideration and favorable action are respectfully solicited.

Respectfully submitted,

  
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If the Examiner is unable to reach the Applicant(s) Attorney at the telephone number provided, the Examiner is requested to communicate with Eastman Kodak Company Patent Operations at (585) 477-4656.

**Amendments to the Drawings:**

Formal drawings are submitted herewith under Separate Letter to the Draftsperson. For the convenience of the Examiner, a copy of the formal drawings are also attached with this amendment.